AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus for memory error control coding comprising:

a first circuit configured to generate a first syndrome signal in response to a read data signal and a read parity signal;

a bypass circuit configured to generate a second syndrome signal in response to said first syndrome signal and a bypass signal, wherein said bypass circuit comprises one or more logic gates configured to (i) receive said first syndrome signal at a first input, (ii) receive said bypass signal at a second input and (iii) present said second syndrome signal at an output; and

a second circuit configured to (i) detect an error when bits of said second syndrome signal are not all the same state and (ii) generate an error location signal in response to said second syndrome signal, wherein said error location signal (i) is generated in response to fewer than all of said bits of said second syndrome signal and (ii) describes a location of a single bit error detected in said read data and parity signals.

2. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein all bits of said first syndrome signal are at a particular state when no error is detected in said read data and parity signals and said particular state comprises a digital 1.

3. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to present said read data and parity signals at an output when no error is detected in said read data and parity signals.

4. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, further comprising a memory circuit configured to (i) receive a data input signal and a parity input signal during a write operation and (ii) present said read data and parity signals during a read operation.

5. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said second circuit is configured to generate (i) a single error signal when a single bit error is detected in said read data and parity signals, (ii) a double error signal when an error is detected in two bits of said read data and parity signals, and (iii) an error detected signal when either said single error signal or said double error signal are generated in response to said second syndrome signal.

6. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, further comprising a corrector circuit configured to generate a corrected representation of said read data and parity signals in response to said error location signal when a single bit error is detected.

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said second circuit is configured to invert each of said bits of said second syndrome signal.

8. (ORIGINAL) The apparatus according to claim 1, further comprising:

an encoder circuit configured to generate said parity signal in response to a data input signal, wherein said encoder circuit comprises a type selected from the group consisting of (i) non-inverting exclusive-OR gates, (ii) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (iii) inverting exclusive-OR gates, (iv) inverting exclusive-OR gates with an output inverted by a NOT gate, (v) non-inverting exclusive-NOR gates, (vi) inverting exclusive-NOR gates, (vii) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, and (viii) inverting exclusive-NOR gates with an output inverted by a NOT gate.

9. (CURRENTLY AMENDED) The apparatus according to claim ~~1~~5, wherein said second circuit comprises:

one or more OR gates configured to receive an inverse of said second syndrome signal and present said error detected signal;

one or more exclusive-OR gates configured to receive an inverse of said second syndrome signal and present an intermediate signal;

one or more AND gates configured to present said single error signal in response to said error detected signal and said intermediate signal; and

an AND gate configured to present said double error signal in response to said error detected signal and an inverse of said intermediate signal.

10. (ORIGINAL) The apparatus according to claim 9, wherein said single error signal comprises a multi-bit digital signal.

11. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said first syndrome signal is generated using a type of syndrome encoder selected from the group consisting of (i) non-inverting exclusive-OR gates, (ii) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (iii) inverting exclusive-OR gates, (iv) inverting exclusive-OR gates with an output inverted by a NOT gate, (v) non-inverting exclusive-NOR gates, (vi) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, (vii) inverting exclusive-NOR gates, and (viii) inverting exclusive-NOR gates with an output inverted by a NOT gate.

12. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said ~~bypass circuit comprises~~ one or more logic gates of said bypass circuit are configured to ~~receive said first syndrome~~

~~signal and said bypass signal, wherein~~ (i) present each of said ~~first~~ bits of said second syndrome signal ~~is presented as~~ having a state determined by a corresponding bit of said ~~second~~ first syndrome signal in response to said bypass signal having a first state and (ii) ~~generation of said error location signal is disabled~~ present all of said bits of said second syndrome signal having the same state in response to said bypass signal having a second state.

13. (PREVIOUSLY PRESENTED) The apparatus according to claim 12, wherein said one or more logic gates are selected from the group consisting of AND, NAND, NOR, and OR gates.

14. (CURRENTLY AMENDED) An apparatus for memory error control coding comprising:

means for generating a first syndrome signal in response to a read data signal and a read parity signal;

means for generating a second syndrome signal in response to said first syndrome signal and a bypass signal, wherein (i) each bit of said second syndrome signal has a state determined by a corresponding bit of said first syndrome signal when said bypass signal is in a first state and (ii) all bits of said second syndrome signal have the same state when said bypass signal is in a second state; and

means for (i) detecting an error when bits of said second syndrome signal are not all the same state and (ii) generating an error location signal in response to said second syndrome signal,

wherein said error location signal (i) is generated in response to fewer than all of said bits of said second syndrome signal and (ii) describes a location of a single bit error detected in said read data and parity signals.

15. (CURRENTLY AMENDED) A method for memory error detection and correction comprising the steps of:

(A) generating a first syndrome signal in response to a read data signal and a read parity signal;

(B) generating a second syndrome signal in response to said first syndrome signal and a bypass signal, wherein (i) each bit of said second syndrome signal has a state determined by a corresponding bit of said first syndrome signal when said bypass signal is in a first state and (ii) all bits of said second syndrome signal have the same state when said bypass signal is in a second state;

(C) detecting an error when bits of said second syndrome signal are not all the same state; and

(D) generating an error location signal in response to said second syndrome signal, wherein said error location signal (i) is generated in response to fewer than all of said bits of said second syndrome signal and (ii) describes a location of a single bit error detected in said read data and parity signals.

16. (PREVIOUSLY PRESENTED) The method according to claim 15, wherein all of said bits of said second syndrome signal are at

a particular state when no error is detected in said read data and parity signals and said particular state comprises a digital 1.

17. (PREVIOUSLY PRESENTED) The method according to claim 15, further comprising the step of:

bypassing said error location signal generating step in response to a predetermined state of said bypass signal.

18. (PREVIOUSLY PRESENTED) The method according to claim 15, wherein step (C) further comprises the sub-steps of:

generating a single error signal when a single bit error is detected in said read data signal or parity signal;

generating a double error signal when an error is detected in two bits of said read data signal or parity signal; and

generating an error detected signal when either said single error signal or said double error signal are generated in response to said second syndrome signal.

19. (PREVIOUSLY PRESENTED) The method according to claim 15, further comprising the step of:

presenting said read data and parity signals when no error is detected in said read data and parity signals.

20. (PREVIOUSLY PRESENTED) The method according to claim 15, further comprising the step of:

generating a corrected representation of said read data and parity signals in response to said error location signal when said single bit error is detected.

21. (CURRENTLY AMENDED) The apparatus according to claim 12, wherein said bypass circuit is configured to present all of said bits of said second syndrome signal ~~having the same state~~ as a digital 1 in response to said bypass signal having said second state.

22. (CURRENTLY AMENDED) An apparatus for memory error control coding comprising:

a syndrome encoder circuit configured to generate a syndrome signal in response to a read data signal and a read parity signal, wherein said syndrome encoder circuit comprises a type of syndrome encoder selected from the group consisting of (i) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (ii) inverting exclusive-OR gates, (iii) inverting exclusive-OR gates with an output inverted by a NOT gate, (iv) non-inverting exclusive-NOR gates, (v) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, (vi) inverting exclusive-NOR gates, and (vii) inverting exclusive-NOR gates with an output inverted by a NOT gate; and

a second circuit configured to (i) detect an error when bits of said syndrome signal are not all the same state and (ii) generate an error location signal in response to said syndrome

signal, wherein said error location signal (i) is generated in response to fewer than all of said bits of said ~~second~~ syndrome signal and (ii) describes a location of a single bit error detected in said read data and parity signals.

23. (CURRENTLY AMENDED) The apparatus according to claim 22, wherein said second circuit comprises:

one or more OR gates configured to receive a complement of said syndrome signal and present ~~said~~ an error detected signal;

one or more exclusive-OR gates configured to receive a complement of said syndrome signal and present an intermediate signal;

one or more AND gates configured to present ~~said~~ a single error signal in response to said error detected signal and said intermediate signal; and

an AND gate configured to present ~~said~~ a double error signal in response to said error detected signal and an inverse of said intermediate signal.